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METHOD OF MARGINAL ERASURE FOR THE TESTING OF FLASH MEMORIES

This application is a Continuation in Part of US Patent Application serial number 10/056,978, filed 1/25/02, now abandoned, which is herein incorporated by reference.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention generally relates to a method used in semiconductor memory manufacturing and, more particularly, to a method of erasing memory cells during testing in a flash electrically erasable programmable read only memory (EEPROM) in the fabrication of integrated circuits (ICs).

(2) Description of Prior Art

Electrically erasable EEPROMs, often referred to as "Flash" EPROM, have emerged as an important non-volatile memory. Having the same cell density as standard EPROMs, they have the advantage over EPROMs that they need not be exposed to ultraviolet (UV) light to be erased. This is also an advantage in that standard IC packages can be used for these devices whereas standard EPROMs require a special package allowing the IC die to be exposed to UV light.

In a standard Flash EPROM, a plurality of flash memory cells are arranged in an array of rows and columns. Refer now to Fig. 1 showing a typical flash memory cell device. Each cell 10 is composed of a p-type substrate 12 and separate n-type source 14